Output impedance

Ideal output would maintain \( V_{OUT, \text{ideal}} \) no matter what.

Real life:

\[
\begin{align*}
\text{Vout, ideal} & \quad \Rightarrow \quad \text{Model any output... ... as:} \\
\text{Vout} & \quad \Rightarrow \quad \text{A} \quad \Rightarrow \quad \text{Iout}
\end{align*}
\]

\[ Z_{OUT} = -\frac{\Delta V_{OUT}}{\Delta I_{OUT}} \]

(low \( Z_{OUT} \) is desirable)

Input impedance

Ideal input would draw no current no matter what: \( I_{IN} \)

Real life:

\[
\begin{align*}
\text{IN} & \quad \Rightarrow \quad \text{Model any input... ... as:} \\
\text{VIN} & \quad \Rightarrow \quad \text{B}
\end{align*}
\]

\[ Z_{IN} = \frac{\Delta V_{IN}}{\Delta I_{IN}} \]

(high \( Z_{IN} \) is desirable)

Loading effects

When \( Z_{IN} \) & \( Z_{OUT} \) are finite, there is a voltage reduction called "loading" due to the voltage divider formed by \( Z_{IN} \) & \( Z_{OUT} \):

\[
\begin{align*}
\text{Ideal A} \quad Z_{OUT} & \quad \Rightarrow \quad \text{Ideal B} \\
\text{VOUT, ideal} & \quad \Rightarrow \quad \frac{Z_{IN}}{Z_{IN} + Z_{OUT}}
\end{align*}
\]

\[
\begin{align*}
\text{VOUT} & = V_{OUT}, \quad \frac{Z_{IN}}{Z_{IN} + Z_{OUT}}
\end{align*}
\]
Bipolar transistors

A transistor is a valve for electricity. A small signal applied to the "handle" controls the main flow of electricity.

**NPN**
- Collector
  - Electron flow
  - $I_c$ (main flow)
- Emitter
  - $I_e$
- Base
  - $I_b$

**PNP**
- Collector
  - Hole flow
  - $I_c$ (main flow)
- Emitter
  - $I_e$
- Base
  - $I_b$

Circuit symbol
- How it looks to a DMM
- Actual construction

Simple model (works most of the time)

1) Be junction is forward-biased in normal operation
   \[ V_{be} \approx 0.6V \] (e.g., for NPN, \[ V_e \approx V_b - 0.6V \])

2) $I_c = \beta I_b$, $\beta \approx 100$ (highly variable, temp. sensitive)

First important circuits w/ bipolar transistors:

**The Emitter Follower**

- $V_{cc}$ (usually +15V)
- $V_{in}$
- $V_{out}$

By rule 1, $V_{out} = V_{in} - 0.6V$.

**Common Emitter Amplifier**

$\Delta V_b = \Delta V_{in}$ (in goes thru C)

$\Delta V_e = \Delta V_b$ (by 1)

$\Delta I_c = \Delta V_e / R_c = \Delta V_{in} / R_{c}$

$\Delta V_{out} = -\Delta I_c R_c$

$V_{cc}$
- $V_{in}$
- $R_c$
- $R_1$
- $R_2$

* $R_1, R_2$ are chosen to
  - $V_{in}$:
    - Set the quiescent operating $V_b$ halfway between 0.6V & $V_{cc}$.
  - $C$ is chosen to block the DC level of $V_{in}$, but allow through signals at frequencies of interest:
    \[ f_{3dB} = \frac{1}{2 \pi R_{11} C} \]
    \[ R_{11} = \frac{R_1 R_2}{R_1 + R_2} \]

\[ V_b \]

\[ V_{out} \]

\[ V_{cc} \]