Lab 5: High-Level Sequential Circuits

Review Questions (optional, not to be handed in)

- Build two circuits to show how to step through through \( n \) timing signals, for \( n = 4 \). In other words, you should send a True signal out along each of \( n \) wires in turn, moving to the next with each clock tick (the other wires should all be False). After the clock cycle in which the last wire is True, the circuit should start over on the first wire. Also include a “synchronous reset” line that makes the next clock tick cause the circuit to start over at the first wire. One of your circuits should be designed using low-level design techniques, and the other high-level — which works better for this problem and why?

- Create a four-bit Gray-code counter in each of the following ways, and describe the advantages/disadvantages of each:
  
a) With a ripple counter and binary-to-gray converter

b) By building a 16-row table and using low-level sequential design.

c) By using a high-level design that could work for any number of bits (this may not be easy).

- Compare your Gray-code counter from step (c) above to a standard four-bit counter (as in Figure 5.32 on Page 254), in terms of (a) the total number of gates, (b) the length of the longest path through the (combinatorial part of) the circuit, and (c) how many the times the combinational part of each circuit could have a gate switch its output (from True to False or vice-versa) after a single clock tick — you should find the maximum total for all output switches of all gates, for each kind of counter. How does a four-bit ripple counter for standard binary numbers compare to these circuits?

- Questions 5-7 and 5-17 from Chapter 5 of Mano’s “Computer Engineering” book.

Circuits (Lab Work)

Obtain the (empty) files for cs240 Lab #5, and do the following (creating a file for each part):

a) Show how a 2\( n \)-bit shift register can be made from two \( n \)-bit shift registers (illustrating for \( n = 2 \)).

b) Show how a 2\( n \)-bit ripple counter can be made from two \( n \)-bit ripple counters (illustrating for \( n = 2 \)).

c) Solve the “vending machine problem” of Lab 4 Question c by using high-level components, trying to minimize the number of 1-bit wires in your system, except for the inputs and outputs, which should be indentical to those of 4c. Include a comment comparing your answers to 4c and this question in terms of the number of bits of state information, the number of gates used outside of the state information, and the length of the longest path through the combinational part of each circuit.